METHOD OF MAKING VERTICAL CHANNEL MASK ROM

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to semiconductor memory devices and more particularly to vertical ROM devices.

2. Description of Related Art

U.S. Pat. No. 5,244,824 of Sivan for "Trench Capacitor and Transistor Structure and Method for Making the Same" shows a vertical channel memory cell for a DRAM.

Current flat type cells need to use a virtual ground technique to reduce effective cell size. Some problems with using such a virtual ground technique are as follows:

1) increase in chip size due to extra decoder circuits required for the virtual ground technique.

2) slower speed results from the additional delays caused by extra decoder circuits.

SUMMARY OF THE INVENTION

An object of this invention is to eliminate the need for a virtual ground technique while maintaining the same cell size as a flat cell for the same layout rule.

In accordance with this invention a method is provided for manufacture of a semiconductor device on a semiconductor substrate. The following sequence of steps is employed. Form an N+ source layer on the surface of the semiconductor substrate. Form a dielectric layer on the surface of the source layer. Pattern and etch the dielectric layer forming a dielectric layer pattern with openings therein. Form a silicon epitaxial layer in the openings in the dielectric layer pattern. Form an N+ drain layer on the surface of the silicon epitaxial layer. Form a second dielectric layer on the surface of the device including the N+ drain layer. Form and pattern a conductor layer containing silicon over the second dielectric layer. Form an N+ implant mask with an N+ opening over a region of the epitaxial layer (source) and ion implanting through that N+ opening into the N+ implant mask in that region. Form a code implant mask over the conductor layer. Ion implant through the code implant mask into the device.

The following are preferred features of the invention. The conductor layer comprises a material selected from polysilicon and a polycide selected from the group consisting of WSi_2, $TiSi_2$, $CoSi_2$, $MoSi_2$, and $TaSi_2$. A dose of boron ions is implanted through the code implant mask into the device. The dose comprises boron ions implanted within the range from about 1E13 cm^{-2} to about 5 E14 cm^{-2}. The dose can be applied at from about 100 keV to about 200 keV. Form an N+ drain layer on the surface of the silicon dielectric layer is performed by ion implant of an N+ dopant, or by thermal deposition and annealing. Form an N+ source layer on the surface of the semiconductor substrate by ion implanting of N+ dopant, preferably arsenic, within the range from 1 E15 cm^{-2} to 8 E15 cm^{-2}. Form an N+ drain layer on the surface of the silicon dielectric layer by thermal diffusion or by ion implanting an N– dopant which can be performed by implanting arsenic ions.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other aspects and advantages of this invention are explained and described below with reference to the accompanying drawings, in which:

FIG. **1** shows a device in the early stages of manufacture comprising a P– silicon substrate on the surface of which an N+ source region has been formed by either one of two processes comprising thermal diffusion or ion implantation.

FIG. **2** shows the device of FIG. **1** with a blanket thermally grown, dielectric, silicon dioxide (thermal oxide) layer formed upon which a mask is then formed.

FIG. **3** shows the device of FIG. **2** after etching through openings in the mask leaving stacks of thermal "oxide" layer on the bottom and "oxide" layer on the top, between which are newly grown silicon epitaxial regions.

FIG. **4** shows the device of FIG. **3** subsequent to formation of N+ drains **30**.

FIG. **5** shows the device of FIG. **4** subsequent to an etching step which removes the remainder of silicon dioxide layer followed by a conventional gate oxide process, and formation of.

FIG. **6** shows the device of FIG. **5** after a polycide (silicon containing), word line (**WL1**) conductor layer **34** is deposited and patterned into word line conductors.

FIG. **7** shows a sectional view of the device of FIG. **6** taken through a source N+ interconnect structure where contact between metallization and the source layer is to be formed by ion implantation of a contact region of the source layer with N+ boron ions.

FIG. **8** shows the device of FIG. **6** covered with a photoresist mask to form a source P-epi code implant mask for making a code implant into channels below and onto the P-epi region which is the channel area of a ROM cell.

FIG. **9** shows an electrical schematic diagram of a device in accordance with this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

This invention provides a new vertical channel memory cell technology employing an epitaxial process for growing a vertical channel. The cell is especially well adapted for use as a Mask ROM and is also adapted to use in other kinds of memories and repeated arrays.

FIG. **1** shows a device **20** in the early stages of manufacture comprising a P– silicon substrate **21** on the surface of which an N+ source region **22** has been formed by either one of two processes comprising:

1) thermal diffusion of arsenic, antimony or phosphorous, or

2) ion implantation of arsenic, antimony or phosphorous with energy at a level from about 60keV to about 120keV, with a dose of 1 E15 cm^{-2} to about 8 E15 cm^{-2} and then thermally annealed.

It should be noted that substrate **21** can be an N– silicon substrate.

FIG. **2** shows the device of FIG. **1** with a blanket thermally grown, dielectric, silicon dioxide (thermal oxide) layer **24** formed having a thickness of from about 100 Å to about 1000 Å by a process selected from the following:

1) dry or steam thermal oxidation at a temperature from 800° C. to 1,000° C.,

2) any chemical vapor deposition (CVD) process for forming silicon dioxide, or

3) a combination of 1) or 2) above with a preference for thermal oxidation.

Next, a blanket, dielectric, silicon dioxide (oxide) layer **26** having a thickness of from about 2,000 Åto about 9,000 Å, which is formed by the process of